IN THE CLAIMS:

Please amend Claims 1, 3, 6, 7, 8, 13, 15, 17, 20, 21, 22, 27, 28, 30 and 38 to 42 as shown below. The claims, as currently pending in the application, read as follows:

1. (Currently Amended) A protocol data unit switching method used for the selective interconnection of a transmitter port and a plurality of receiver ports selected from among at least two receiver ports by means of at least one internal bus, said protocol data units being constituted by at least one elementary piece of data, wherein the method comprises:

a synchronization mechanism defining time slots, called connection cycles, on ~~at least one of~~ said internal ~~buses~~ bus;

a mechanism for the allocation of at least one of said connection cycles to each of the selected receiver ports; and

a mechanism for the writing of at least one piece of elementary data in the allocated connection cycle or cycles so as to enable the broadcasting of the protocol data unit to said selected receiver ports,

wherein said writing mechanism comprises a verification step determining whether all the elementary pieces of data constituting [[the]] a current protocol data unit have been received by each of the selected receiver ports,

and wherein writing of at least one elementary piece of data belonging to another protocol data unit to any one of the selected receiver ports [[are]] is blocked until all ~~of them~~ the selected receiver ports have received all the elementary pieces of data constituting the current protocol data unit.

2. (Canceled)

3. (Currently Amended) A method according to claim 1, wherein said writing mechanism is reiterated for any not-yet-serviced selected receiver port, so long as all the elementary pieces of data constituting the current protocol data unit have not been received by said ~~not-yet-serviced~~ not-yet-serviced selected receiver port.

4. (Previously Presented) A method according to claim 1, wherein said allocation mechanism comprises a step of association of each of said connection cycles to each of said selected receiver ports.

5. (Previously Presented) A method according to claim 1, wherein said allocation mechanism comprises:

a step for the detection of a transmitter port requesting the transfer of at least one protocol data unit towards at least one selected receiver port;

a step for verifying that the selected receiver port or ports are ready to receive the protocol data unit or units; and

a step for the validation of at least one connection cycle used for the writing of the elementary data of the protocol data unit or units in the selected receiver ports during the validated connection cycle or cycles when the verification is positive.

6. (Currently Amended) A method according to claim 1, further comprising:

multiplexing on at least one ~~first~~ input bus ~~multiplexing~~ the elementary pieces of data coming from ~~at least two ports among said receiver ports and~~ a plurality of transmitter ports ~~and/or~~ and addressed to a first subset of the at least two receiver ports; and

multiplexing on at least one ~~first~~ output bus ~~multiplexing~~ the elementary pieces of data coming from ~~at least two ports among said receiver ports and~~ said plurality of transmitter ports and addressed to a second subset of the at least two receiver ports.

7. (Currently Amended) A method according to claim 1, wherein ~~said~~ transmitter and receiver ports are organized in pairs each combining a transmitter port and a receiver port, each pair being associated with a distinct link.

8. (Currently Amended) A method according to claim 1, further comprising at least one link connected to said transmitter port ~~ports~~ and/or to said receiver ports.

9. (Previously Presented) A method according to claim 8, wherein the link belongs to the group comprising:

IEEE 1355 or equivalent links; and

external buses.

10. (Canceled)

11. (Previously Presented) A method according to claim 1, wherein said writing mechanism comprises at least one step for the writing of each piece of elementary data of each of said protocol data units, each of said steps for writing each piece of elementary data comprising:

a sub-step for the acceptance, by each of said selected receiver ports, of the writing of each piece of elementary data to be transmitted; and

a sub-step for the transmission of said each piece of elementary data to be transmitted, to each of said selected receiver ports.

12. (Previously Presented) A method according to claim 11, wherein during said acceptance sub-step, the acceptance is conditioned by a degree of filling of a reception memory associated with said selected receiver port, for each of said receiver ports.

13. (Currently Amended) A method according to claim 1, wherein said writing mechanism comprises at least one step of arbitration for at least one bus connecting a set of at least one input port comprising said transmitter port to a set of at least one output port comprising said receiver ports, said arbitration step being carried out by a switching matrix consisting of crosspoints capable of managing the transmission of elementary data between an input port and an output port, and being organized in rows and columns,

each column, or row respectively, ~~(or row respectively)~~ being capable of managing the reception of elementary data coming from an input port associated with the column, or row respectively; ~~(or row respectively);~~ and

each row, or column respectively, ~~(or column respectively)~~ being capable of managing the transmission of elementary data to an output port associated with the row, or column respectively; ~~(or column respectively);~~

so that a single crosspoint per row, or column respectively, ~~(or column respectively)~~, at a given point in time, can enable the transmission of elementary data.

14. (Previously Presented) A method according to claim 1, wherein each protocol data unit transmitted comprises at least one routing header and wherein the method further comprises:

at least one step for the analysis of said routing header; and/or

at least one step for the modification of said routing header.

15. (Currently Amended) A protocol data unit switching device which selectively interconnects a transmitter port and a plurality of receiver ports selected from at least two receiver ports by means of at least one internal bus, said protocol data units being constituted by at least one piece of elementary data, wherein the device comprises:

a synchronization unit which defines time slots, called connection cycles, on ~~at least one of~~ said internal ~~buses~~ bus;

an allocation unit which allocates at least one of the connection cycles to each of the selected receiver ports; and

a writing unit which writes at least one piece of elementary data in the allocated connection cycle or cycles, so as to enable the broadcasting of the protocol data unit to the selected receiver ports,

wherein said writing unit comprises a verification unit determining whether all the elementary pieces of data constituting [[the]] a current protocol data unit have been received by each of the selected receiver ports,

and wherein writing of at least one elementary piece of data belonging to another protocol data unit to any one of the selected receiver ports [[are]] is blocked until all ~~of them~~ the selected receiver ports have received all the elementary pieces of data constituting the current protocol data unit.

16. (Canceled)

17. (Currently Amended) A device according to claim 15, wherein said writing unit is activated for any not-yet-serviced selected receiver port, so long as all the elementary pieces of data constituting the current protocol data unit have not been received by said not-yet-serviced selected receiver port.

18. (Previously Presented) A device according to claim 15, wherein said allocation unit associates each of said connection cycles to each of said selected receiver ports.

19. (Previously Presented) A device according to claim 15, wherein said allocation unit performs:

detection of a transmitter port requesting the transfer of at least one protocol data unit towards at least one selected receiver port;

verification that the selected receiver port or ports are ready to receive the protocol data unit or units; and

validation of at least one connection cycle used for the writing of the elementary data of the protocol data unit or units in the selected receiver ports during the validated connection cycle or cycles when the verification is positive.

20. (Currently Amended) A device according to claim 15, further comprising: [[;]]

at least one ~~first~~ input bus multiplexing the elementary pieces of data coming from a plurality of transmitter ports and addressed to a first subset of the at least two ~~ports among said~~ receiver ports; and ~~and transmitter ports, and/or~~

at least one ~~first~~ output bus multiplexing the elementary pieces of data coming from said plurality of transmitter ports and addressed to a second subset of the at least two ~~ports among said~~ receiver ~~ports and transmitter~~ ports.

21. (Currently Amended) A device according to claim 15, wherein ~~said~~ transmitter and receiver ports are organized in pairs, each combining a transmitter port and a receiver port, each pair being associated with a distinct link.

22. (Currently Amended) A device according to claim 15, further comprising at least one link connected to said transmitter port ~~ports~~ and/or to said receiver ports.

23. (Previously Presented) A device according to claim 22, wherein the link belongs to the group comprising:

IEEE 1355 or equivalent links; and

external buses.

24. (Canceled)

25. (Previously Presented) A device according to claim 15, wherein said writing unit writes each piece of elementary data of each of said protocol data units, and:

accepts, by each of the selected receiver ports, of the writing of said each piece of elementary data to be transmitted, and

transmits said each piece of elementary data to be transmitted, to each of the selected receiver ports.

26. (Previously Presented) A device according to claim 25, wherein the acceptance implemented by said writing unit is conditioned by a degree of filling of a reception memory associated with the selected receiver port, for each of said receiver ports.

27. (Currently Amended) A device according[[,]] to claim 26, wherein said reception memory comprises at least one FIFO.

28. (Currently Amended) A device according to claim 15, wherein said writing unit arbitrates at least one bus connecting a set of at least one input port comprising said transmitter port to a set of at least one output port comprising said receiver ports, the arbitration step is carried out by a switching matrix consisting of crosspoints capable of managing the transmission of elementary data between an input port and an output port, and organized in rows and columns,

each said column, or row respectively, ~~(or row respectively)~~ being capable of managing the reception of elementary data coming from an input port associated with the column, or row respectively; ~~(or row respectively);~~ and

each said row, or column respectively, ~~(or column respectively)~~ being capable of managing the transmission of elementary data to an output port associated with the row, or column respectively; ~~(or column respectively);~~

so that a single crosspoint per row, or column respectively, ~~(or column respectively),~~ at a given point in time, can enable the transmission of pieces of elementary data.

29. (Previously Presented) A device according to claim 15, wherein each protocol data unit transmitted comprises at least one routing header and the device further comprises:

at least one unit for the analysis of said routing header; and/or

at least one unit for the modification of said routing header.

30. (Currently Amended) A device according to claim 15, further comprising an interfacing unit for delivering, to a control module and through a clock signal transmission unit, clock signals regenerated from packets received by said interfacing unit.

31. (Previously Presented) A device according to claim 15, further comprising an interfacing unit for transmitting and/or receiving information through at most two connection buses addressed to and/or coming from at least one of the means belonging to the group comprising said synchronization unit, said allocation unit and said writing unit.

32. (Previously Presented) A device according to claim 31, wherein the protocol data units sent out by at least one emitter port towards FIFOs are multiplexed by a reception linking bus.

33. (Previously Presented) A device according to claim 31, wherein the protocol data units received by at least one receiver port through the FIFOs are demultiplexed on a transmission linking bus.

34. (Previously Presented) A switching apparatus comprising:

at least one switching device according to claim 15; and

at least one element belonging to the group comprising:

IEEE 1355 or equivalent links, and

external buses.

35. (Previously Presented) A switching apparatus according to claim 34, connected to a data processing apparatus.

36. (Previously Presented) A method according to claim 1, wherein the method is applied to at least one of the fields belonging to the group comprising:

high bit rate switching;

distributed applications;

the transmission of digital data;

the reception of digital data;

audio applications;

company networks; and

real-time image transmission.

37. (Canceled)

38. (Currently Amended) A computer program stored on a computer-readable medium, the program executing a protocol data unit switching method used for the selective interconnection of a transmitter port and a plurality of receiver ports selected from at least two receiver ports by means of at least one internal bus, said protocol data unit being constituted by at least one elementary piece of data, the program comprising:

[[-]]a synchronization step defining time slots, called connection cycles, on ~~at least one of~~ the internal ~~buses~~ bus;

[[-]]an allocation step for the allocation of at least one of the connection cycles to each of said selected receiver ports; and

[[-]]a writing step for the writing of at least one piece of elementary data in the allocated connection cycle or cycles so as to enable the broadcasting of the protocol data unit to said selected receiver ports, said writing step comprising a verification step determining whether all the elementary pieces of data constituting [[the]] a current protocol data unit have been received by each of the selected receiver ports, and writing of at least one elementary piece of data belonging to another protocol data unit to any one of the selected receiver ports being blocked until all ~~of them~~ the selected receiver ports have received all the elementary pieces of data constituting the current protocol data unit.

39. (Currently Amended) A method according to claim 13, wherein at least one column, or row respectively, ~~(or row respectively)~~ of said switching matrix comprises at least two crosspoints each associated with a different receiver port, so that at a given point in time a same piece of elementary data can be transferred to the at least two receiver ports associated with said at least two crosspoints.

40. (Currently Amended) A method according to claim 39, wherein the switching means comprises N receiver ports, and wherein at least one column, or row respectively, ~~(or row respectively)~~ of said switching matrix comprises N crosspoints each

associated with one of the N receiver ports, so that at a given point in time a same piece of elementary data can be transferred to the N receiver ports.

41. (Currently Amended) A device according to claim 28, wherein at least one column, or row respectively, ~~(or row respectively)~~ of said switching matrix comprises at least two crosspoints each associated with a different receiver port, so that at a given point in time a same piece of elementary data can be transferred to the at least two receiver ports associated with said at least two crosspoints.

42. (Currently Amended) A device according to claim 41, wherein the switching means comprises N receiver ports, and wherein at least one column, or row respectively, ~~(or row respectively)~~ of said switching matrix comprises N crosspoints each associated with one of the N receiver ports, so that at a given point in time a same piece of elementary data can be transferred to the N receiver ports.